IN THE CLAIMS

This listing of claims will replace all prior versions and listings of claims in the application:

LISTING OF CLAIMS:

1. (Currently Amended) A method for fabricating a capacitor of a semiconductor device, comprising the steps of:

forming sequentially a lower electrode and a dielectric layer having a high dielectric constant over a semiconductor substrate which ~~have~~ has gone through predetermined processes;

forming sequentially a first metal layer and a poly-silicon layer over the dielectric layer;

forming an upper electrode pattern by ~~pattering~~ patterning the poly-silicon layer and the first metal layer;

forming a second metal layer covering the upper electrode pattern on ~~an entire surface of~~ the semiconductor substrate; and

forming an upper electrode constituted with the second metal layer, the poly-silicon layer and the first metal layer by patterning the second metal layer so that the second metal layer is connected ~~with~~ to the first metal layer.

2. (Original) The method as recited in claim 1, wherein a titanium nitride (TiN) layer is used for forming the first metal layer.

3. (Original) The method as recited in claim 2, wherein the TiN layer is formed by performing a chemical vapor deposition (CVD) process.

4. (Original) The method as recited in claim 3, wherein a thickness of the TiN layer ranges from about 100 Å to about 500 Å.

5. (Currently Amended) The method as recited in claim 1, wherein the second metal layer is constituted with one of ~~such layers as~~ a titanium nitride (TiN) layer, a titanium (Ti) layer, a tungsten (W) layer and an aluminum (Al) layer.

6. (Original) The method as recited in claim 5, wherein a thickness of the second metal layer ranges from about 100 Å to about 1000 Å.

7. (Original) The method as recited in claim 1, wherein a thickness of the poly-silicon layer ranges from about 300 Å to about 2500 Å.

8. (Currently Amended) The method as recited in claim 1, wherein the dielectric layer is constituted with one of ~~such layers as~~ a tantalum oxide (Ta_2O_5) layer, a titanium oxide (TiO_2) layer, an aluminum oxide (Al_2O_3)-tantalum oxide (Ta_2O_5)

double layer, strontium titanium oxide ($SrTiO_3$) layer and a piezoelectric translator (PZT) layer.

9. (Currently Amended) The method as recited in claim 1, further comprising the steps of:

forming an inter-layer insulation film on the semiconductor substrate after forming the upper electrode; and

forming a contact hole exposing a portion of the upper electrode by etching the inter-layer insulation film.

10. (New) A method for fabricating a capacitor of a semiconductor device, comprising the steps of:

forming sequentially a lower electrode and a dielectric layer having a high dielectric constant over a semiconductor substrate;

forming sequentially a first metal layer and a poly-silicon layer over the dielectric layer;

forming an upper electrode pattern by patterning the poly-silicon layer and the first metal layer;

forming a second metal layer covering the upper electrode pattern on the semiconductor substrate; and

patterning the second metal layer to form an upper electrode consists of the patterned second metal layer, the patterned poly-silicon layer and the patterned first metal layer

so that the patterned second metal layer is electrically connected to the patterned first metal layer.

11. (New) The method as recited in claim 10, wherein a titanium nitride (TiN) layer is used for forming the first metal layer.

12. (New) The method as recited in claim 11, wherein the TiN layer is formed by performing a chemical vapor deposition (CVD) process.

13. (New) The method as recited in claim 12, wherein a thickness of the TiN layer ranges from about 100 Å to about 500 Å.

14. (New) The method as recited in claim 10, wherein the second metal layer is constituted with one of a titanium nitride (TiN) layer, a titanium (Ti) layer, a tungsten (W) layer and an aluminum (Al) layer.

15. (New) The method as recited in claim 14, wherein a thickness of the second metal layer ranges from about 100 Å to about 1000 Å.

16. (New) The method as recited in claim 10, wherein a thickness of the poly-silicon layer ranges from about 300 Å to about 2500 Å.

17. (New) The method as recited in claim 10, wherein the dielectric layer is constituted with one of a tantalum oxide (Ta_2O_5) layer, a titanium oxide (TiO_2) layer, an aluminum oxide (Al_2O_3)-tantalum oxide (Ta_2O_5) double layer, strontium titanium oxide ($SrTiO_3$) layer and a piezoelectric translator (PZT) layer.

18. (New) The method as recited in claim 10, further comprising the steps of:

forming an inter-layer insulation film on the semiconductor substrate after forming the upper electrode; and

forming a contact hole exposing a portion of the upper electrode by etching the inter-layer insulation film.